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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,961	12/19/2001	Shunpei Yamazaki	740756-2410	7583

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,961	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) *1-5,23-27 and 45-65* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-22 and 28-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/19/01,4/3/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS filed 11/25/02*.

DETAILED ACTION

This Office Action is in response to the amendment and election. Currently, claims 1-65 are pending. The Specie I (figures 1A-1C), that are readable on claims 6-22, and 28-44 have been elected.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 12/19/01, 4/03/02, and 11/25/02. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-22 and 28-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makita et al., US Patent 5,821,562 in view of Henley et al., US Patent 6,683,324.

4. Makita discloses the semiconductor method substantially as claimed. See figures 1-29, with emphasis on figures 8A-8H, an corresponding text, where Makita shows, pertaining to claims 6, 12, 17 and 28, a method of manufacturing a semiconductor device comprising the steps

of: adding a metal element to a semiconductor film having an amorphous structure (figure 8A; col. 18, lines 20-67; col. 19, lines 1-38); crystallizing semiconductor film by a first heat treatment to form a crystalline semiconductor film (figure 8A-D; col. 19, lines 13-45); irradiating the crystalline semiconductor with laser light to improve crystallinity (figure 8E; col. 19, lines 46-53; claims 6 and 17); forming mask insulating film having an opening on the crystalline semiconductor film (figures 8A-8C; col. 19, lines 1-38; claims 28, 34, and 39); forming an impurity region in the crystalline semiconductor film (figure 8C; col. 19, lines 24-38); and segregating the metal element in the impurity region by a second heat treatment (figure 8C; col. 19, lines 24-38); and removing the impurity region by etching (figure 8D; col. 19, lines 39-45; claims 12, 17, 34, and 39). In addition, Makita shows, pertaining to claims 7, 13, and 18, a method of manufacturing a semiconductor device, wherein the first heat treatment is performed by a rapid thermal anneal method using one heat source selected from the group consisting of halogen lamp, a metal halide lamp, a xenon arc lamp, and a carbon arc lamp (col. 21, lines 38-48). Also, pertaining to claims 8 and 19, Makita shows, a method of manufacturing a semiconductor device, wherein the laser light is emitted using one selected from the group consisting of an excimer laser, a YAG laser, a YVO_4 laser, or a YLF laser(col. 21, lines 38-48). Pertaining to claims 9, 14, and 20, Makita shows, a method of manufacturing a semiconductor device, wherein the second heat treatment is performed by a rapid thermal anneal method using one heat source selected from the group consisting of a halogen lamp, a metal halide lamp, a xenon arc lamp, and a carbon arc lamp (col. 21, lines 38-48). In addition, pertaining to claims 10, 15, and 21, Makita shows, a method of manufacturing a semiconductor device, wherein the

metal element is at least one selected from the group consisting of Fe, Ni, Co, Ru, Pd, Os, Ir, Pt, Cu, and Au (col. 19, lines 7-12).

5. However, Makita fails to show, pertaining to claims 6, 11, 12, 16, 17, 22, 28, 31, 34, 39 and 44, forming an impurity region to which a noble gas element (an ion of a noble gas element accelerated by an electric field)) is added in the crystalline semiconductor film (through the opening), wherein the noble gas element is at least one selected from the group consisting of helium, neon, argon, krypton, and xenon. In addition, Makita fails to show, removing the impurity region containing the noble gas element (an ion of a noble gas element) by etching.

6. Henley teaches, on figures 1A-9C, with emphasis on figures 6A-7, and corresponding text, a polycrystalline silicon layer or an amorphous silicon layer may be used as a gettering layer were noble gas ions are implanted into the layer, and an annealing method is performed (col. , lines 1-4, lines 21-47; col. 3, lines 60-64; col. 4, lines 42-45; col. 7, lines 54-67; col. 8, lines 1-29)

7. It would have been obvious to one of ordinary skill in the art to substitute, forming an impurity region to which a noble gas element (an ion of a noble gas element accelerated by an electric field)) is added in the crystalline semiconductor film (through the opening). In addition, removing the impurity region containing the noble gas element (an ion of a noble gas element) by etching, pertaining to claims 6, 12, 17, 28, 34, and 39, in the method of Makita, according to the teachings of Henley, with the motivation of, removing the impurities for example, metals, such as copper, nickel, siliver, gold, or iron, from the active device region, for the purpose of producing a contamination free active region. Therefore, it would be obvious to one of ordinary skill in the art to add a noble gas element to the crystalline semiconductor film and then remove

the impurity region containing the noble gas by etching, for the purpose of removing the metal element implanted within the crystallized semiconductor film where the noble gas element is has been implanted.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY PATENT EXAMINER
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Stanetta Isaac
Patent Examiner
November 29, 2004